

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

GS 162 D1

Application Number

Unassigned

Applicant(s)

Richard A. Blanchard

Filing Date

Filed Herewith

Group Art Unit

2826

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TL	1	5,744,719A	04-1998	Werner	73	514.32	
	2	5,895,951 A	04-1999	So et al.	257	330	
	3	6,184,555 B1	02-2001	Tihanyi et al.	257	342	
	4	5,216,275	6-1993	Chen	257	493	
	5	5,404,040	4-1995	Hshieh et al.	257	341	
	6	5,973,360	10-1999	Tihanyi	257	330	
	7	4,959,699	9-1990	Lidow et al.	357	23.7	
TL	8	US-20020070418 A1	06-2002	Kinzer et al.	257	491	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
TL	1	DE 198 00 647 C1	5/27/99	Germany	H01L29	78		✓
	2	DE 197 48 523 A1	5/12/99	Germany	H01L29	78		✓
	3	WO 99/23703	3/14/99	PCT	H01L29	06		✓
	4	EP 0 053 854 B1	5/2/86	EPO	H01L29	06	✓	
TL	5	EP 0 973 203 A2	1/19/00	EPO	H01L29	06		✓

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

1	G. Deboy et al. "A New Generation of High Voltage MOSFETS Breaks The Limit Line of Silicon," Electron Devices Meeting, San Francisco, California, December 6-9 1998, Paper No. 26.2.1, pgs. 683-685, Sponsored by Electron Devices Society of IEEE.
2	T. Fujihira et al., "Simulated Superior Performances of Semiconductor Superjunction Devices," Proceedings of 1998 International Symposium on Power Semiconductor Devices & ICs, Kyoto, Japan, pp. 423-426.

EXAMINER

DATE CONSIDERED

12/08/04.

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Use several sheets if necessary)

GS 162 D1

Unassigned

Richard A. Blanchard

Filed Herewith

2826

*EXAMINER
INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Jean-Marie Peter, "Power Semiconductors: New Devices Pursue Lower On-Resistance, Higher Voltage Operation," PCIM, January 1999, pp. 26-32.

5

"Power Semiconductors Proliferate: Expanding Product Lines and Advancing Process Technology Promise Higher Performance in Varied Applications," *Electronic Products*, July 1999, pp. 23-24.

6

L. Lorenz et al., "Improved MOSFET: An Important Milestone Toward A New Power MOSFET Generation," PCIM, September 1998, pp. 14-22.

7

X. Chen, "Optimum Design Parameters For Different Patterns of CB-Structure," Chinese Journal of Electronics, Vol. 9, No. 1, January 2000, pp. 6-11.

8

Jack Glenn et al., "A Novel Vertical Deep Trench RESURF DMOS (VTR-DMOS)," *Proceedings of the 12th International Symposium on Power Semiconductor Devices & ICS*, Toulouse, France, May 22-25, 2000, pp. 197-200.

9

EXAMINER

DATE CONSIDERED

***EXAMINER:** Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

